CLAIM AMENDMENTS

Claims 1-22 *(CANCELLED)*

23. *(NEW)* A method for suspending operation of a pipelined data processor to reduce power consumption, comprising:

enabling a first clock signal in response to an occurrence of a first combination of respective states of one or more clock control signals;

advancing a sequence of instructions to a first portion of a pipeline subcircuit;

executing said advanced sequence of instructions with a second portion of said pipeline subcircuit subsequent to said first pipeline subcircuit portion in response to said enabled first clock signal; and

detecting an occurrence of a second combination of said respective states of said one or more clock control signals and in response thereto

interrupting said advancing of said sequence of instructions to said first pipeline subcircuit portion, followed by

executing with said second pipeline subcircuit portion a plurality of microcode substantially unrelated to said sequence of instructions in response to said enabled first clock signal, and followed further by

disabling said first clock signal.

24. *(NEW)* The method of claim 23, further comprising:

retrieving said sequence of instructions from a first portion of memory prior to said advancing of said sequence of instructions; and

retrieving said plurality of microcode from a second portion of said memory prior to said executing of said plurality of microcode.

25. *(NEW)* The method of claim 23, further comprising:

retrieving said sequence of instructions from a first portion of memory prior to

said advancing of said sequence of instructions; and

retrieving said plurality of microcode from a second portion of said memory following said interrupting of said advancing of said sequence of instructions and prior to said executing of said plurality of microcode.

26. *(NEW)* The method of claim 23, wherein:

retrieving said sequence of instructions from a first memory circuit prior to said advancing of said sequence of instructions; and

retrieving said plurality of microcode from a second memory circuit prior to said executing of said plurality of microcode.

27. *(NEW)* The method of claim 23, wherein:

retrieving said sequence of instructions from a first memory circuit prior to said advancing of said sequence of instructions; and

retrieving said plurality of microcode from a second memory circuit following said interrupting of said advancing of said sequence of instructions and prior to said executing of said plurality of microcode.

28. *(NEW)* The method of claim 23, further comprising generating said plurality of microcode with circuitry including said pipeline subcircuit.

29. *(NEW)* The method of claim 23, further comprising:

generating, with said pipeline subcircuit in response to said enabled first clock signal, a plurality of data corresponding to said executing of one of said advanced sequence of instructions and plurality of microcode; and

retaining, with said pipeline subcircuit, said plurality of data in response to said disabled first clock signal.

30. *(NEW)* The method of claim 23, further comprising, prior to said

executing of said plurality of microcode, completing executing of one or more of said advanced sequence of instructions which had been advanced to said first pipeline subcircuit portion prior to said detection of an occurrence of said second combination of said respective states of said one or more clock control signals.

31. *(NEW)* The method of claim 30, further comprising:

generating, with said pipeline subcircuit in response to said enabled first clock signal, a plurality of data corresponding to said executing of one of said advanced sequence of instructions and plurality of microcode; and

retaining, with said pipeline subcircuit, said plurality of data in response to said disabled first clock signal.

32. *(NEW)* The method of claim 23, further comprising, following said interrupting of said advancing of said sequence of instructions to said first pipeline subcircuit portion and prior to said executing of said plurality of microcode, completing executing of one or more of said advanced sequence of instructions which had been advanced to said first pipeline subcircuit portion prior to said interrupting of said advancing of said sequence of instructions to said first pipeline subcircuit portion.

33. *(NEW)* The method of claim 23, further comprising detecting another occurrence of said first combination of said respective states of said one or more clock control signals and in response thereto re-enabling said first clock signal.

34. *(NEW)* The method of claim 33, further comprising:

resuming said advancing of said sequence of instructions to said first pipeline subcircuit portion; and

resuming said executing of said advanced sequence of instructions with said second pipeline subcircuit portion in response to said re-enabled first clock signal.

35. *(NEW)* The method of claim 23, further comprising asserting a status signal indicative of said disabling of said first clock signal.

36. *(NEW)* The method of claim 35, further comprising, following said executing of said plurality of microcode, monitoring an operating status of a coprocessor associated with said pipeline subcircuit prior to said asserting of said status signal, and wherein said asserting a status signal indicative of said disabling of said first clock signal comprises asserting said status signal following an indication that said coprocessor operating status is in a selected state.

37. *(NEW)* The method of claim 23, further comprising, following said executing of said plurality of microcode, monitoring an operating status of a coprocessor associated with said pipeline subcircuit prior to said disabling of said first clock signal, and wherein said disabling said first clock signal comprises disabling said first clock signal following an indication that said coprocessor operating status is in a selected state.

38. *(NEW)* The method of claim 23, further comprising:

generating a second clock signal; and

maintaining said second clock signal in an enabled state substantially independently of said disabling of said first clock signal.

39. *(NEW)* A method for suspending operation of a pipelined data processor to reduce power consumption, comprising:

enabling a first clock signal in response to an occurrence of a first combination of respective states of one or more clock control signals;

advancing a sequence of instructions to a first portion of a pipeline subcircuit;

executing said advanced sequence of instructions with a second portion of said

pipeline subcircuit subsequent to said first pipeline subcircuit portion in response to said enabled first clock signal; and

detecting an occurrence of a second combination of said respective states of said one or more clock control signals and in response thereto

interrupting said advancing of said sequence of instructions to said first pipeline subcircuit portion, followed by

generating a plurality of address data and

executing with said second pipeline subcircuit portion a plurality of microcode corresponding to said plurality of address data and substantially unrelated to said sequence of instructions in response to said enabled first clock signal, and followed further by

disabling said first clock signal.

40. *(NEW)* The method of claim 39, further comprising:

retrieving said sequence of instructions from a first portion of memory prior to said advancing of said sequence of instructions; and

retrieving said plurality of microcode from a second portion of said memory prior to said executing of said plurality of microcode.

41. *(NEW)* The method of claim 39, further comprising:

retrieving said sequence of instructions from a first portion of memory prior to said advancing of said sequence of instructions; and

retrieving said plurality of microcode from a second portion of said memory following said interrupting of said advancing of said sequence of instructions and prior to said executing of said plurality of microcode.

42. *(NEW)* The method of claim 39, wherein:

retrieving said sequence of instructions from a first memory circuit prior to said advancing of said sequence of instructions; and

retrieving said plurality of microcode from a second memory circuit prior to said executing of said plurality of microcode.

43. *(NEW)* The method of claim 39, wherein:

retrieving said sequence of instructions from a first memory circuit prior to said advancing of said sequence of instructions; and

retrieving said plurality of microcode from a second memory circuit following said interrupting of said advancing of said sequence of instructions and prior to said executing of said plurality of microcode.

44. *(NEW)* The method of claim 39, further comprising generating said plurality of microcode with circuitry including said pipeline subcircuit.

45. *(NEW)* The method of claim 39, further comprising:

generating, with said pipeline subcircuit in response to said enabled first clock signal, a plurality of data corresponding to said executing of one of said advanced sequence of instructions and plurality of microcode; and

retaining, with said pipeline subcircuit, said plurality of data in response to said disabled first clock signal.

46. *(NEW)* The method of claim 39, further comprising, prior to said executing of said plurality of microcode, completing executing of one or more of said advanced sequence of instructions which had been advanced to said first pipeline subcircuit portion prior to said detection of an occurrence of said second combination of said respective states of said one or more clock control signals.

47. *(NEW)* The method of claim 46, further comprising:

generating, with said pipeline subcircuit in response to said enabled first clock signal, a plurality of data corresponding to said executing of one of said advanced

sequence of instructions and plurality of microcode; and

retaining, with said pipeline subcircuit, said plurality of data in response to said disabled first clock signal.

48. *(NEW)* The method of claim 39, further comprising, following said interrupting of said advancing of said sequence of instructions to said first pipeline subcircuit portion and prior to said executing of said plurality of microcode, completing executing of one or more of said advanced sequence of instructions which had been advanced to said first pipeline subcircuit portion prior to said interrupting of said advancing of said sequence of instructions to said first pipeline subcircuit portion.

49. *(NEW)* The method of claim 39, further comprising detecting another occurrence of said first combination of said respective states of said one or more clock control signals and in response thereto re-enabling said first clock signal.

50. *(NEW)* The method of claim 49, further comprising:

resuming said advancing of said sequence of instructions to said first pipeline subcircuit portion; and

resuming said executing of said advanced sequence of instructions with said second pipeline subcircuit portion in response to said re-enabled first clock signal.

51. *(NEW)* The method of claim 39, further comprising asserting a status signal indicative of said disabling of said first clock signal.

52. *(NEW)* The method of claim 51, further comprising, following said executing of said plurality of microcode, monitoring an operating status of a coprocessor associated with said pipeline subcircuit prior to said asserting of said status signal, and wherein said asserting a status signal indicative of said disabling of

said first clock signal comprises asserting said status signal following an indication that said coprocessor operating status is in a selected state.

53. *(NEW)* The method of claim 39, further comprising, following said executing of said plurality of microcode, monitoring an operating status of a coprocessor associated with said pipeline subcircuit prior to said disabling of said first clock signal, and wherein said disabling said first clock signal comprises disabling said first clock signal following an indication that said coprocessor operating status is in a selected state.

54. *(NEW)* The method of claim 39, further comprising:

generating a second clock signal; and

maintaining said second clock signal in an enabled state substantially independently of said disabling of said first clock signal.

55. *(NEW)* A method for suspending operation of a pipelined data processor to reduce power consumption, comprising:

enabling a first clock signal in response to an occurrence of a first combination of respective states of one or more clock control signals;

advancing a sequence of instructions to a first portion of a pipeline subcircuit;

executing said advanced sequence of instructions with a second portion of said pipeline subcircuit subsequent to said first pipeline subcircuit portion in response to said enabled first clock signal; and

detecting an occurrence of a second combination of said respective states of said one or more clock control signals and in response thereto

interrupting said advancing of said sequence of instructions to said first pipeline subcircuit portion, followed by

generating a plurality of address data,

addressing said first pipeline subcircuit portion with said plurality of

address data and in response thereto generating a plurality of microcode substantially unrelated to said sequence of instructions, and

executing said plurality of microcode with said second pipeline subcircuit portion in response to said enabled first clock signal, and followed further by

disabling said first clock signal.

56. *(NEW)* The method of claim 55, further comprising:

retrieving said sequence of instructions from a first portion of memory prior to said advancing of said sequence of instructions; and

retrieving said plurality of microcode from a second portion of said memory prior to said executing of said plurality of microcode.

57. *(NEW)* The method of claim 55, further comprising:

retrieving said sequence of instructions from a first portion of memory prior to said advancing of said sequence of instructions; and

retrieving said plurality of microcode from a second portion of said memory following said interrupting of said advancing of said sequence of instructions and prior to said executing of said plurality of microcode.

58. *(NEW)* The method of claim 55, wherein:

retrieving said sequence of instructions from a first memory circuit prior to said advancing of said sequence of instructions; and

retrieving said plurality of microcode from a second memory circuit prior to said executing of said plurality of microcode.

59. *(NEW)* The method of claim 55, wherein:

retrieving said sequence of instructions from a first memory circuit prior to said advancing of said sequence of instructions; and

retrieving said plurality of microcode from a second memory circuit following said interrupting of said advancing of said sequence of instructions and prior to said executing of said plurality of microcode.

60. *(NEW)* The method of claim 55, further comprising:

generating, with said pipeline subcircuit in response to said enabled first clock signal, a plurality of data corresponding to said executing of one of said advanced sequence of instructions and plurality of microcode; and

retaining, with said pipeline subcircuit, said plurality of data in response to said disabled first clock signal.

61. *(NEW)* The method of claim 55, further comprising, prior to said executing of said plurality of microcode, completing executing of one or more of said advanced sequence of instructions which had been advanced to said first pipeline subcircuit portion prior to said detection of an occurrence of said second combination of said respective states of said one or more clock control signals.

62. *(NEW)* The method of claim 61, further comprising:

generating, with said pipeline subcircuit in response to said enabled first clock signal, a plurality of data corresponding to said executing of one of said advanced sequence of instructions and plurality of microcode; and

retaining, with said pipeline subcircuit, said plurality of data in response to said disabled first clock signal.

63. *(NEW)* The method of claim 55, further comprising, following said interrupting of said advancing of said sequence of instructions to said first pipeline subcircuit portion and prior to said executing of said plurality of microcode, completing executing of one or more of said advanced sequence of instructions which had been advanced to said first pipeline subcircuit portion prior to said interrupting of

said advancing of said sequence of instructions to said first pipeline subcircuit portion.

64. *(NEW)* The method of claim 55, further comprising detecting another occurrence of said first combination of said respective states of said one or more clock control signals and in response thereto re-enabling said first clock signal.

65. *(NEW)* The method of claim 64, further comprising:

resuming said advancing of said sequence of instructions to said first pipeline subcircuit portion; and

resuming said executing of said advanced sequence of instructions with said second pipeline subcircuit portion in response to said re-enabled first clock signal.

66. *(NEW)* The method of claim 55, further comprising asserting a status signal indicative of said disabling of said first clock signal.

67. *(NEW)* The method of claim 66, further comprising, following said executing of said plurality of microcode, monitoring an operating status of a coprocessor associated with said pipeline subcircuit prior to said asserting of said status signal, and wherein said asserting a status signal indicative of said disabling of said first clock signal comprises asserting said status signal following an indication that said coprocessor operating status is in a selected state.

68. *(NEW)* The method of claim 55, further comprising, following said executing of said plurality of microcode, monitoring an operating status of a coprocessor associated with said pipeline subcircuit prior to said disabling of said first clock signal, and wherein said disabling said first clock signal comprises disabling said first clock signal following an indication that said coprocessor operating status is in a selected state.

69. *(NEW)* The method of claim 55, further comprising:

generating a second clock signal; and

maintaining said second clock signal in an enabled state substantially independently of said disabling of said first clock signal.